**“A Taste of Data path + Control Design Example: Factorial Circuit (Open Ended Lab)”**

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**Spring 2024**

## CSE-308L

### Digital System Design Lab

Submitted by: **Naveed Ahmad** Registration No.: **22PWCSE2165**

Class Section: **B**

“I affirm that I have completed this work with integrity”

Student Signature:

Submitted to:

### Engr. Shah Zada Fahim Jan

Sunday, June 1, 2025

Department of Computer Systems Engineering

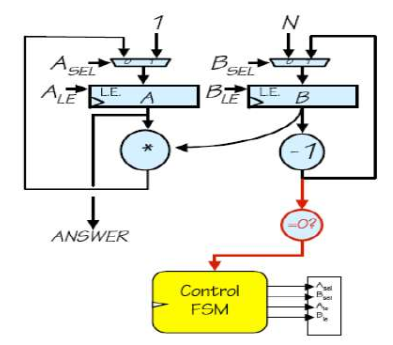
University of Engineering and Technology, Peshawar

**Lab Objectives**

To implement a circuit that calculates factorial of a number.

**Block Diagram:**

The datapath for computing the factorial of an N-bit number is shown below. It operates under the control of a Finite State Machine (FSM), which generates the control signals Asel, Ale, Bsel, and Ble at appropriate times to manage the datapath operations. The FSM receives an input signal Z; when Z = 0, it indicates that the computation is complete and the result (ANSWER) can be read. The corresponding State Transition Graph (STG) is also provided in the diagram.

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**A screenshot of a computer

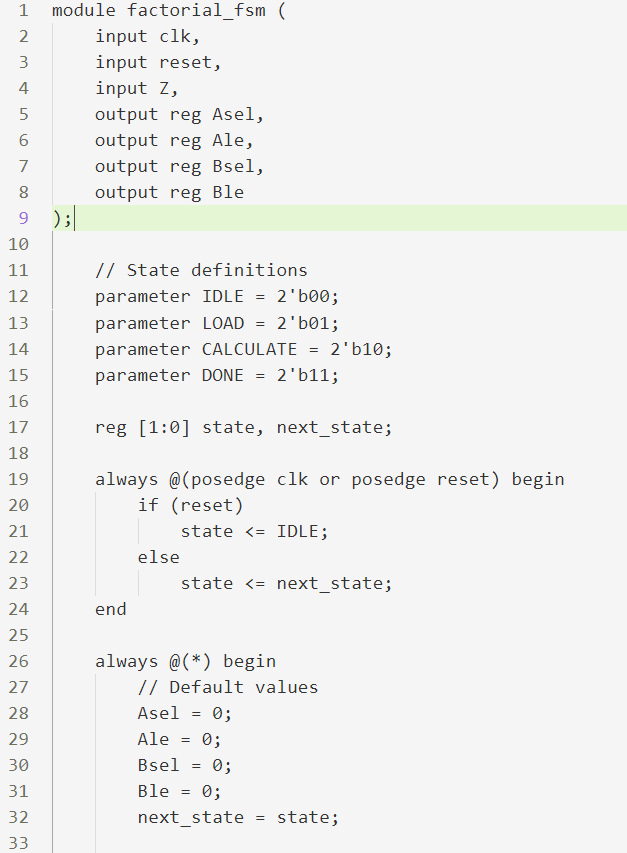
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**Lab Task**

**TASK:1**

Module file:

Factorial Fsm Module:



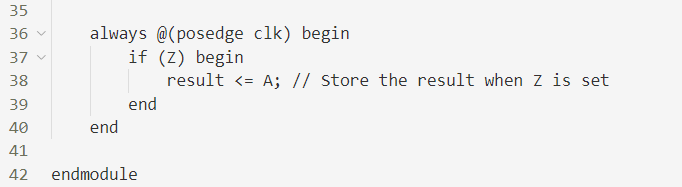
A screenshot of a computer program

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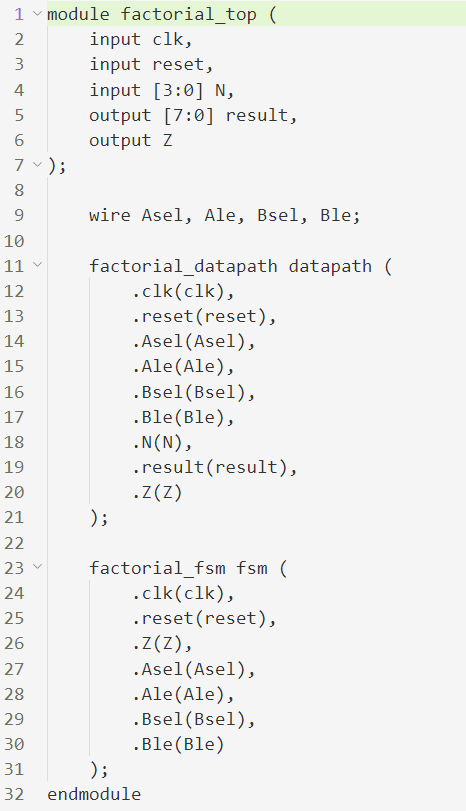
Datapath Module:

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Top Module:



Test Bench Module:

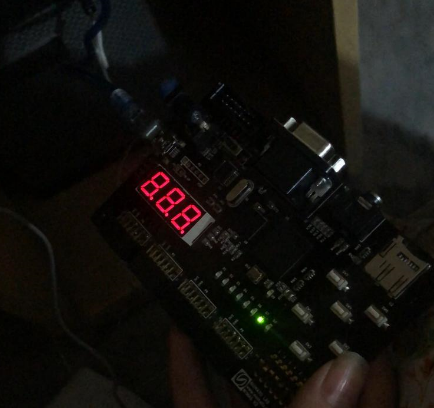
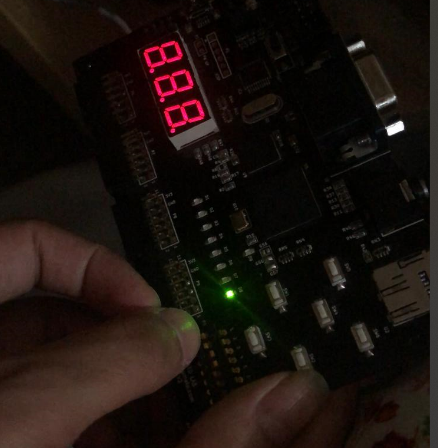
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Output:

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**OUTPUT:**

